Department of Electronics Communication Engineering

Andhra University College of Engineering

Visakhapatnam-530003

2 years M.Tech (VLSI & EMBEDDED SYSTEMS)

Scheme of Instruction and Examination with Effect from 2023-2024 Admitted Batch Onwards

Under AICTE Curriculum

I SEMESTER

Subject Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVE1.1	RTL Simulation and Synthesis with PLDs	3	-	70	30	100	3
MTVE1.2	Embedded Systems	3	-	70	30	100	3
MTVE1.3	Elective – I Digital Design through Verilog/ VLSI Testing / Programming Languages for Embedded Software	3	-	70	30	100	3
MTVE1.4	Elective – II System Design with Embedded Linux/ VLSI Signal Processing/ CAD of VLSI Systems	3	-	70	30	100	3
MTVE1.5	Research Methodology & IPR	3	-	70	30	100	2
MTVE1.6	Audit Course	3	-	-	100	100	0
MTVE1.7	RTL Simulation and Synthesis with PLDs Lab	-	3	-	100	100	2
MTVE1.8	Embedded Systems Lab	-	3	-	100	100	2
	Total	18	6	350	450	800	18

II SEMESTER

Subject Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVE2.1	VLSI Design Verification and Testing	3	-	70	30	100	3
MTVE2.2	Communication Buses and Interfaces	3	-	70	30	100	3
MTVE2.3	Elective – III Physical Design Automation/ Memory Technologies/ SOC Design	3	-	70	30	100	3
MTVE2.4	Elective – IV Low Power VLSI Design/ DSP Architecture/ Analog and Digital CMOS/ VLSI Design	3	-	70	30	100	3
MTVE2.5	Audit Course	3	-	-	100	100	0
MTVE2.6	VLSI Design Verification and Testing Lab		3	-	100	100	2
MTVE2.7	Analog and Digital CMOS VLSI Design Lab	-	3	-	100	100	2
MTVE2.8	Mini Project with Seminar	-	3	-	100	100	2
	Total	15	9	280	520	800	18

III SEMESTER

Subject Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVE3.1	Elective – V Optimization Techniques/ Bio medical Signal Processing/ Internet of Things and Applications	3	-	70	30	100	3
MTVE3.2	Open Elective Waste as a source of energy/ Operations Research/ Composite materials	3	-	70	30	100	3
MTVE3.3	Dissertation- I / Industrial Project	-	-	-	100	100	10
	Total	6	-	140	160	300	16

IV SEMESTER

Subject Code	Name of the Subject	Periods/Week		Max. Marks		Total	Credits
		Theory	Lab	Ext.	Int.		
MTVE 4.1	Dissertation- II	-	-	100	0	100	16
	Total	-	-	100	0	100	16

AUDIT COURSE 1 & 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills.

RTL SIMULATION AND SYNTHESIS WITH PLDs
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.1	**L**	**P**	**C**
I-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Describe Finite State Machines and comprehend concepts of clock related issues.
CO2: Model digital circuits using Verilog and understand the concepts of clock related issues. Mixed signal Systems design using Verilog AMS.
CO3: Outline the concepts of different design flows in VLSI.
CO4: Illustrate different low power latches and Flip-flops.
CO5: Explain the concepts of IP cores and Prototyping.

UNIT-I
DESIGN STRATEGIES
Top-down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

UNIT-II
MODELING OF DIGITAL CIRCUITS
Design entry by Verilog, Combinational and sequential Logic Design: Multiplexer/DE-multiplexer, ALU, parity circuits, Flip-flops, shift Register, Counters, Finite State Machines, Sequence generator, Sequence detector, Verilog AMS.

UNIT-III
DESIGN METHODOLOGIES
Programmable Logic Devices, FPGA, SoC, Introduction to ASIC Design Flow, Floor Planning, Placement, Clock tree synthesis, Routing, Physical verification.

UNIT- IV
LOW POWER LATCHES AND FLIP-FLOPS
Introduction, Need for lower latches and flip-flops, Evolution of Latches and Flip-flops, Quality measures for latches and flip-flops, Design perspective.

UNIT-V
IP AND PROTOTYPING
IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Net list, Physical IP, use of external hard IP during prototyping.

TEXT BOOKS
1. Richard S. Sandige, Modern Digital Design, MGH, International Editions, 1990
2. T. R. Padmanabhan and B.F.V.G. Bala Tripura Sundari, Design through Verilog HDL, WSE, IEEE Press, 2004.

3. Zeidman, Bob. Designing with FPGAS and CPLDS. CRC Press, 2002.
4. KiatSeng Yeo, Samir S. Rafail, Wang-Ling Goh, CMOS/Bi CMOS ULSI Low Voltage Low Power, Pearson Education Asia 1st Indian reprint, 2002.
5. Doug Amos, Austin Lesea, Rene Richter, FPGA based prototyping methodology manual, Xilinx.

REFERENCES

1. Palnitkar, Samir. Verilog HDL: a guide to digital design and synthesis. Pearson Education India, 2003.
2. Givone, Donald D. Digital principles and design. Palgrave Macmillan, 2003.
3. Roth, Charles H.Digital systems design using VHDL. Wadsworth Publ. Co., 1998.

EMBEDDED SYSTEMS
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.2	**L**	**P**	**C**
I-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUT COMES: At the end of the course the student will be able to

C01: Summarize ARM Instructions set.

C02: Identify pipeline, Thumb instructions.

C03: Compare and select several features /peripherals of SOC LPC 29X.

C04: Describe knowledge about Cortex-M3 Operations.

CO5: Analyze Cortex Interrupts.

UNIT-I

ARM INSTRUCTIONS

ARM Architecture, ARM 9,32/16-bit ARM instructions set, Data Transfer, Bit clear, Masking, Arithmetic, logic instructions, Data and Bit Manipulations.

UNIT-II

PIPELINING and THUMB INSTRUCTIONS

Pipelining: 3 Stage and 5 stage, Exception handling, Thumb instructions set: Thumb bit, Branch and data processing instructions, single register and multiple register data transfer Instructions.

UNIT -III

LPC 29XX PERIPHERALS

LPC 29XX peripherals LPC 29xx features, Timers, ADC, URAT, I2C, SPI, PWM, APB, GPIOs, ARM Development tools, JTAG boundary scan test architecture.

UNIT –IV

CORTEX –M3 INSTRUCTINS AND MAP

ARM Cortex –M3 processor: Programming model, Registers, Operation model, Interrupts, Reset Sequence Instructions set, Memory Maps, Memory Access, Attributes, Permissions, Big- Band Operations, Unaligned and Exclusive Transfer.

UNIT-V

INTERRUPTS VECTOR AND SEQUENCE

Vector Tables, interrupts inputs and pending behavior, Fault Exceptions, Supervisor service Call, Nested vectored interrupt Controller, Basic Configuration, SYSTICK timer, Interrupt sequence, Exists, Interrupt Latency.

TEXT BOOKS

1. Kamal, Raj. Microcontrollers: Architecture, Programming. Interfacing and System Design. Pearson Education India, 2011.
2. Stephen Bo, ARM system-on- chip architecture. Pearson Education, 2000.
3. Yiu, Joseph, The definitive guide to the ARM Cortex – M3. Newens, 2009.

4. Technical references and user manuals from NXP Semiconductor www.nxp.com

REFERENCES

1. Das, Lyla Embedded systems: An Integrated Approach. Pearson Education India, 2012.
2. Prasad, Dr. KVKK. Embedded/Real-Time systems- Concepts, Design & Programming - Black book. 2010.

Elective-I
DIGITAL DESIGN THROUGH VERILOG
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.3	**L**	**P**	**C**
I-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Outline the basic concepts of Verilog language
CO2: Design and develop different circuits in gate level modeling
CO3: Develop circuits in data flow level modeling and switch level modeling
CO4: Design different circuits in behavioral modeling using blocking and non-blocking Statements
CO5: Design Finite states machines and comprehends concepts of functions, tasks, and user Defined primitives

UNIT- I
INTRODUCTION TO VERILOG
Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verifications, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches. Language Constructs and Conventions: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators. System Tasks and Functions, File-Based Tasks and Functions, Compiler Directive, Hierarchical Access, General Observations.

UNIT-II
GATE LEVEL MODELING
Introduction, AND Gate Primitive, Module Structure, Other Gate Primitive, Illustrative Examples, Tri-state Gates, Array of Instances of Primitives, Additional Examples, Design of Flip-flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits.

UNIT-III
DATA FLOW LEVEL and SWITCH LEVEL MODELING
Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignments to Vectors, Operators. Switch Level Modeling Introduction, Basic Transistors Switches, CMOS Switch, Bidirectional Gates, Time Delays with Switch Primitives, Instantiations with Strength and Delays, Strength Contention with Trireg Nets.

UNIT-IV

BEHAVIOUR MODELING

Introduction, Operators and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Examples, Assignments with Delays, Wait construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non-blocking Assignments, The case statement, Simulation Flow. If and if-else constructs, assign-reassign construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

UNIT-V

FUNCTIONS, TASKS AND USER-DEFINED PRIMITIVES

Introduction, Function, recursive functions, Tasks, User Defined Primitives (UDP) combinational UDPs, FSM Design-Moore and Mealy Machines.

TEST BOOKS

1. T. R. Padmanabhan and B. Bala Tripura Sundari, Design through Verilog HDL, WSE, IEEE Press, 2004

2. Bhaskar, Jayaram. A Verilog HDL Primer, Star Galaxy Publishing, 1999.

REFERENCES

1. Michael D. Ciletti, Advanced Digital Design with Verilog HDL, PHL, 2005.

2. John F. Wakerly, Digital Design Principles & Practices, PHL/Pearson Education Asia, 3rd Ed.

Elective-I
VLSI TESTING
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.3	**L**	**P**	**C**
I-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Analyze the need for fault modeling and testing of digital circuits
CO2: Describe test generation for combinational Logic circuits
CO3: Summarize test generation for Sequential circuits
CO4: Illustrate design of testable sequential circuits using scan path and non-scan path
CO5: Design of Built in Self-test for RAM chip

UNIT-I
FAULTS AND LOGIC SIMULATION
Faults in digital circuits: Failures and Faults, Modeling of faults, Temporary Faults. Logic Simulation: Applications, Problems in simulation based design verification, types of simulation, The unknown logic values, complied simulation, event-driven simulation, Delay models, Element evaluation, Hazard detection, Gate-level event-driven simulation.

UNIT-II
FAULT DIAGNOSIS AND TESTING
Test generation for combinational Logic circuits: Fault Diagnosis of digital circuits, Test generation techniques for combination circuits, detection of multiple faults in combinational logic circuits. Testable combinational logic circuit design-I: The Read- Muller, expansion technique, three level OR-AND-OR design, Automatic synthesis of testable logic.

UNIT-III
TESTING OF LOGIC CIRCUITS
Testable Combinational logic circuit design –II: Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design. Test generation for Sequential circuits: Testing of Sequential circuits as Iterative combinational circuits, state table verification, Test generation based on circuit structure, functional fault models, test generation on function fault models.

UNIT-IV
DESIGN OF TESTABLE SEQUENTIAL CIRCUITS
Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive scan design(LSSD), Random Access scan technique, Partial scan, testable sequential circuit design using Nonscan techniques, cross check , Boundary scan.

UNIT-V
FAULT DIAGNOSIS OF MEMORIES

Built-In self-test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures. Testable Memory Design: RAM Fault Models, test algorithms for RAMs, detection of pattern –sensitive faults, BIST techniques for RAM chips, test generation and BIST for embedded RAMs.

TEXT BOOKS

1. LalaParag K, Digital Circuit Testing and Testability, New York, Academic Press, 1997.
2. Abramovici M, Breuer MA and Friedman A D, Digital Systems Testing and Testable Design, Wiley, 1994

REFERENCES

1. Vishwani D Agarwal, Essential of Electronic Testing for Digital, Memory and Mixed signal Circuits, Springer, 2002.
2. Wang, Wu and Wen, VLSI Test principles and Architectures, Morgan kaufmann, 2006

Elective-I

PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE

(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.3	**L**	**P**	**C**
I-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the student will be able to

CO1: Develop drivers for low speed peripherals.

CO2: Develop OOPS concepts.

CO3: Develop CPP programing.

CO4: Illustrate Inheritance, overloading concepts.

CO5: Explain PERL scripting.

UNIT-1

EMBEDDED PERIPHERALS

Embedded 'C' Programming, Bitwise operations, Dynamic memory allocation, OS services, Linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code Optimization issues, Writing LED drivers, Drivers for serial port communication, Embedded Software Development and Cycle and Methods (Waterfall, Agile).

UNIT-II

OOPS PROGRAMMING TECHNIQUES

Object Oriented Programing: Introduction to procedural, Modular, Object-Oriented and Generic Programming techniques, Limitations of procedural programming, Objects, Classes, Data members, Methods, Data Encapsulation, Data abstraction and information hiding, Inheritance, Polymorphism.

UNIT-III

MEMORY ALLOCATION TECHNIQUES

CPP Programming: 'cin', 'cout', Formatting and I/O manipulators, New and delete Operators Defining a class, Data members and methods, 'this' pointer, Constructors, Destructors, Friend function, Dynamic memory allocation.

UNIT-IV

OVERLOADING AND INHERITANCE

Need of operator overloading, overloading the assignment, Overloading using friends, Type Conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, Virtual functions.

UNIT-V

TEMPLATES

Function template and class template, member function templates and template arguments, Multiple Exceptions, Scripting Languages, PERL: Operators, Statements Pattern Matching

TEXT BOOKS

1. Michael J. Pont, Embedded C, Pearson Education, 2nd Edition, 2008.
2. Michael Berman, Data structures via C++, Oxford University Press, 2002.
3. Randal L. Schwartz, Learning Perl, O'Reilly Publications, 6th Edition 2011.

REFERENCES

1. Robert Sedgewick, Algorithms in C++, Addison Wesley Publishing Company,1999.
2. Abraham Silberscatz, Peter B, Greg Gange, Operating System Concepts, John Willey & Sons, 2005.

Elective-II
SYSTEM DESIGN WITH EMBEDDED LINUX
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.4	**L**	**P**	**C**
I-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Explain the environment.
CO2: Analyze kernel architecture functions.
CO3: Summarize the embedded drivers.
CO4: Analyze case studies of embedded OS.
CO5: Interpret RT LINUX

UNIT-1
OVERVIEW OF LINUX
Introduction to UNIX/LINUX, LINUX commands, file I/O (open, create, close, Iseek, read, write), process control (fork, vfork, exit, wait, waitpid, exec), Embedded Linux Vs Desktop Linux, Embedded Linux Distributions.

UNIT-II
LINUX KERNEL
Embedded Linux Architecture, Kernel Architecture, Hardware Extraction layer, Memory manager, Scheduler, File System, I/O and networking subsystem, Inter process communication, User space, Start-up sequence.

UNIT-III
EMBEDDED DRIVERS
Board Support Package: Embedded Storage, Memory Technology Devices (MTD), Architecture. Embedded Drivers: Serial, 12C, USB, Ethernet, Timer, Kernel Modules, Embedded File System.

UNIT-IV
BUILDING AND DEBUGGING
Kernel, Root file system, Case studies: RTL LINUX, Micro C/OS-II, Vx Works, Embedded LINUX, Tiny OS.

UNIT-V
LINUX TASKS
Porting Applications, Real-Time Linux basics, Kernel priority, Task creation, print commands, compilation, safety critical features, components, programs.

TEXT BOOKS

1. Prasad, Dr KVKK. Embedded/Real-Time Systems-Concepts, Design & Programming-Black Book. 2010.

2. Yaghmour, Karim. Building embedded Linux system. O'Reilly japan, 2003.

3. Raghavan, pichai, Amol Lad, and Sriram Neelakandan. Embedded Linux system design and development. Auerbach Publication, 2005.

REFERENCES

1. Christopher Hallinan, Embedded Linux Primer: A Practical Real-World Approach, Prentice Hall, 2nd Edition, 2010.

2. Derek Molloy, Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux, Wiley, 1st Edition, 2014.

Elective- II
VLSI SIGNAL PROCESSING
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.4	**L**	**P**	**C**
I-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the coarse the student will be able to
CO1: Explain DSP algorithms, its DFG representation, pipelining and parallel processing approaches.
CO2: Describe iteration bound, retiming techniques.
CO3: Summarize the folding and unfolding algorithms.
CO4: Outline the systolic architecture design.
CO5: Explain different convolution techniques and features of DSP Processor.

UNIT-1
DSP SYSTEMS AND ALGORITHMS
Introduction of DSP systems: Introduction, Overview of typical DSP Algorithms, Representation of DSP Algorithms: Block Diagrams, Signal-Flow Graph, Data-Flow Graph, Dependence Graph. Pipelining and parallel processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing.

UNIT-II
ITERATION BOUND AND RETIMING
Introduction to Iteration bound, Data-Flow Graph Representation, Loop Bound and Iteration Bound, Algorithm for Computing Iteration Bound, Iteration Bound of Multirate Data-Flow Graphs. Introduction to retiming, Definitions and properties, Solving Systems of Inequalities, Retiming Techniques.

UNIT-III
FOLDING AND UNFOLDING
Unfolding: Introduction, an Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming. Folding: Introduction, Folding transformation, Register Minimization Techniques, Register Minimization in Folded Architectures.

UNIT-IV
SYSTOLIC ARCHITECTURE DESIGN
Introduction, systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling vector, Matrix-Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing delays.

UNIT-V
CONVOLUTION AND DIGITAL SIGNAL PROCESSOR
Fast Convolution: Cook-Toom Algorithm, Winograd Algorithm, Iterated Convolution and Cyclic Convolution. Programmable Digital Signal Processors: Introduction & Evaluation of

Programmable Digital Signal Processors, Features of DSP Processors.

TEXT BOOKS

1. Keshab K. Parhi, VLSI Digital signal processing systems, design and implementation, Wiley, Inter Science, 1999.

REFERENCES

1. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGraw Hill, 1994.
2. S.Y. Kung, H.J. White House, T. Kailath, VLSI and modern Signal Processing, Prentice Hall, 1985.

Elective-II
CAD OF VLSI SYSTEM
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.4	**L**	**P**	**C**
I-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Explain the fundamentals of modeling, design, test and verification of VLSI systems
CO2: Describe various phases of CAD including simulation, physical design test, and verification
CO3: Demonstrate knowledge of computational algorithms.
CO4: Summarize about the simulation, synthesis and verification of digital circuit
CO5: Analyze various MCM technologies

UNIT-I
VLSI METHODOLOGIES
Design problem, Design domain, Design action, methods and technologies. Design and Fabrication of VLSI Devices-Fabrication materials, Transistor Fundamentals, Fabrication of VLSI circuits. Fabrication process and its impact on Design –Issues related to fabrication processes, solution for interconnect issues

UNIT-II
VLSI DESIGN AUTOMATION TOOLS
Algorithm and system design, Structural and logic design, transistor level design, layout design verification methods. Data structural and basic algorithms- Data structure for the representation of graphs, graph theory and algorithm like Depth first search, Breadth first search, Dijkstra's shortest path algorithm, Prim's Algorithm for minimum spanning trees, computational complexity, tractable and intractable problems- Combinational optimization problems, Decision problems, complexity classes

UNIT-III
COMBINATIONAL OPTIMIZATION
General purpose methods for combinational optimization, Basic concepts on participating, floor planning and pin assignment, placement, routing algorithms, The Unit- Size placement problem, back tracking and branch and bound, Dynamic programming, integer linear programming, Local search, simulated annealing, Tabu search, Genetic algorithm.

UNIT-IV
SIMULATION AND SYNTHESIS
General remarks on VLSI simulation, Gate level modeling and simulations, Introduction to combinational logic synthesis and verification, Binary decision diagrams, High level Synthesis- hardware models, internal representation of the input algorithm.

UNIT-V

MCM TECHNOLOGIES

MCM physical design cycle, partition, placement-chip array based approach, full custom approach, routing-classification of MCM routing algorithm, maze routing, multiple stage routing, topological routing, integrated pin distribution and routing, routing in programmable multichip modules.

TEXT BOOKS

1. S. H. Gerez, Algorithm for VLSI Design Automation, WILEY student edition, John Wiley &sons (Asia) Pvt.Ltd.1999

2. Naveed Sherwani, Algorithms for VLSI Physical Design Automation, Springer International Edition 3rd Edition, 2005.

REFERENCES

1. Hill &Peterson, computer aided Logical design With emphasis on VLSI, John Wiley, 1993

2. Wayne Wolf, Modern VLSI Design Systems on silicon, Pearson Education Asia, 2nd edition, 1998.

RESEARCH METHODOLODGY & IPR
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.5	**L**	**P**	**C**
I-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Illustrate research problem formulation.
CO2: Analyze research information and research ethics
CO3: Summarize the present-day scenario controlled and monitored by computer and Information Technology, where the future world will be ruled by dynamic ideas, concepts, Creativity and innovation.
CO4: Explain how IPR would take such an important place in growth of individuals & to nation. Summarize the need of information about intellectual property right to be promoted among student community in general & engineering in particular.
CO5: Relate that IPR protection provides an incentive to inventors for further research work and Investment in R & D, which leads to creation of new and better products, and in turn brings about economic growth and social benefits.

UNIT - I
RESEARCH METHODOLOGY: AN INTRODUCTION
Meaning of research problem, Sources of research problem, Criteria and Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

UNIT - II
LITERATURE SURVEY AND ETHICS
Effective literature studies approaches, analysis Plagiarism, and Research ethics.

UNIT - III
INTERPRETATION AND REPORT WRITING
Effective technical writing, how to write a report, Paper Developing a Research Proposal, Format of research proposal, presentation and assessment by a review committee.

UNIT - IV
INTELLECTUAL PROPERTY RIGHTS AND PATENTS
Nature of intellectual Property: Patents, Designs, Trade and copyrights. Process of Patenting and Development: technological research, innovation, patenting, developing. International Scenario: International cooperative on intellectual property, procedure for grants of patents, patenting under PCT.

UNIT - V
INTELLECTUAL PATENT RIGHTS AND DEVELOPMENTS

Scope of patent rights, Licensing and transfer of technology, patent information and databases, Geographical indications. New developments in IPR: Administration of patent system, new development in IPR; IPR of Biological systems, Computer Software etc. Traditional knowledge, case studies, IPR and IITs / NITs/IIITs.

TEXT BOOKS

1. C.R.Kothari, "Research Methodology", 3rd Edition new age international, 2017.
2. Ranjit Kumar," Research Methodology – A Step by step for Beginner s", 2nd Edition, Pearson, Education, 2016.
3. T.Ramappa, "Intellectual Property Rights under WTO", 2nd Edition, S Chand, 2015
4. Kompal Bansal & Parshit Bansal," Fundamentals of IPR for beginner s", 1st Edition, BS Publications, 2016.

REFERENCES

1. Mark Saunders, Philip Levis, Adrain Thornbill, "Research Methods for Business Students", 3rd Edition (Reprint), Pearson Education, 2013.
2. KVS Sharma, "Statistics made simple, Do it yourself", 2ndEdition (Reprint), Prentice Hall, 2010.

MTVE1.6 Audit course

(Refer Annexure-I for Syllabus Details)

RTL SIMULAITON AND SYNTHESIS WITH PLDs LAB
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.7	**L**	**P**	**C**
I-Semester	**0**	**3**	**2**
	Ext. Marks:----		
	Int. Marks: 100		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Design, simulate and synthesize combinational circuits using Verilog.
CO2: Design, simulate and synthesize sequential circuits using Verilog.
CO3: Demonstrate EDA tools like Cadence and Xilinx.
CO4: Develop the digital systems on FPGAs.
CO5: Calculate delay and power for digital circuits using CADENCE software tool.

LIST OF EXPERIMENTS:
1. 8:1 Multiplexer and 1:8 De-multiplexer
2. 4-bit ALU
3. 8-bit Comparator
4. 8-bit Shift Register
5. Sequence Detector
6. Single Port SRAM
7. Universal Asynchronous Receiver/Transmitter (UART)
8. 4 to 16 Decoder
9. BCD Adder
10. CMOS NAND/NOR Gates
11. Parity Checker
12. 8-bit Up/Down Counter
13. Sequence Generator
14. Traffic Light Controller

Note: Any **TWELVE** of the above experiments are to be conducted.

EMBEDDED SYSTEMS LAB
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE1.8	**L**	**P**	**C**
I-Semester	**0**	**3**	**2**
		Ext. Marks:----	
		Int. Marks: 100	

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Explain the control of LED intensity using C program
CO2: Demonstrate low speed external UART communication
CO3: Illustrate ADC operations
CO4: Test on board LCD for various operations
CO5: Examine the DAC operations with I2C/SPI interface

LIST OF EXPERIMENTS
1. Perform basic Arithmetic operations
2. Control intensity of an LED using PWM implemented in software and hardware
3. Control seven segment display
4. Control UART for sending and receiving messages.
5. Control DC motor/Stepper motor
6. Control LCD
7. ADC channel testing with a rotary Potentiometer
8. Control an LED using switch by polling method
9. Test SPI/12C interface
10. Control DAC
11. Control Timer
12. Tasking switching Semaphore
13. Design Pulse Width Modulation
14. Sine wave generator using look-up table method

Note: Any **TWELVE** of the above experiments are to be conducted.

VLSI DESIGN VERIFICATION AND TESTING
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE2.1	**L**	**P**	**C**
II-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Outline the concepts of verification methodologies.
CO2: Explain the concepts of various data types
CO3: Develop test bench environment for Design under test
CO4: Summarize the System Verilog assertions.
CO5: Describe the applications of randomization techniques.

UNIT-I
VERIFICATION GUIDELINES
Verification Process, Basic Test bench functionality, directed testing, Methodology basics, Constrained- Random stimulus, Functional coverage, Test Bench Components Layered test bench, Building layered test bench, Simulation environment phases, Maximum code reuse, Test bench performance.

UNIT - II
DATE TYPES
Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative, Linked listsm, Array methods, choosing a storage type, creating new types with typed, Creating user-defined structures. Type conversion. Enumerated types, Constants, strings, expression width.

UNIT - III
PROCEDURAL STATEMENTS AND ROUTINES
Procedural statements, tasks, functions and void Functions, Routine arguments, returning from routine, local data storage. Time values Connecting the test bench and design: Separating the test bench and design. Interface constructs, Stimulus. Interface driving and sampling, connecting it all together, Top-level scope, Program - Module interactions.

UNIT - IV
SYSTEM VERILOG ASSERTIONS
Basic OOP: Introduction first class, a class OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variable vs. Global variables,, Class routines, Defining routines, outside of the class, Scoping rules. Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Private, Straying off course building a test bench.

UNIT - V
RANDOMIZATION
Introduction, randomization, Randomization in System Verilog, Constraint details, solution probabilities, Controlling multiple constraint blocks, valid constraints, In-time constraints.

The Pre-randomize and Post randomize functions, Constraints tips and techniques, common randomization problems.

TEXT BOOKS

Spear, Chris. System Verilog for verification: a guide to learning the test bench language features, 2nd Edition Springier Science & Business Media, 2008

REFERENCES

1. IEEE 1800-2009 standard (IEEE Standard for System Verilog Unified, Hardware Design, Specification, and Verification Language).
2. System Verilog website: www.systemverilog.org.
3. OVM, UVM (on top of SV) www.verficationacademy.com,

COMMUNICATION BUSES AND INTERFACES
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE2.2	**L**	**P**	**C**
II-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course, the student will be able to:
CO1: Select Low speed Serial buses for various applications
CO2: Demonstrate Low speed serial buses Configuration
CO3: Interpret Automotive Bus Frame structure
CO4: Analyze USE Descriptors
CO5: Describe high speed PCIe bus configuration space

UNIT-I
LOW SPEED SERIAL BUS ARCHITECTURE
Serial Buses RS232, 12C, SPI Features, Frame structure, Control signals, Limitations.

UNIT-II
LOW SPEED SERIAL BUS PHYSICAL INTERFACE
Serial Buses RS232, RS485, 12C, SPI, Physical Interface, Configuration and applications

UNIT-III
CAN ARCHITECTURE
Features, Architecture, Frame structure, Physical Interface, Data transmission, Applications.

UNIT-IV
USB ARCHITECTURE
Transfer types, Enumeration, Descriptor types and contents. Device driver.

UNIT-V
PCIE ARCHITECTURE
Revisions, Features, Configuration space, Hardware protocols, Applications.

TEXT BOOKS
1. Axelson, J. Serial Port Complete: COM Ports, USB Virtual COM Ports, and Ports for Embedded Systems, ser, 2nd Edition, Complete Guides Series. Lakeview Research 2007.
2. Axelson, Jan. USB completes. Lakeview Research, 2015.
3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press
4. Wilfried Voss, A Comprehensible Guide to Controller Area Network, Copperhill Media Corporation, 2nd Edition, 2005.

REFERENCES
1. Serial Front Panel Draft Standard VITA 17.1 – 200x
2. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

Elective-III
PHYSICAL DESIGN AUTOMATION
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE2.3	**L**	**P**	**C**
II-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the students will be able to
CO1: Describe the automation process for VLSI System design
CO2: Explain the fundamentals of physical design
CO3: Develop and enhance the existing algorithm and computational techniques
CO4: Design process of VLSI system
CO5: Illustrate various Routing process and algorithms

UNIT-I
VLSI PHYSICAL DESIGN AUTOMATION
VLSI design cycle, new trends in VLSI design cycle, Physical design cycle, Design styles, System packing styles - Die packing and attachments styles.

UNIT-II
LAYOUT COMPACTION
Standard cell layout, Layout compaction, Design rules, symbolic layout, problem formulation, algorithms for constraint-graph compaction.

UNIT-III
DISCRETE METHODS IN GLOBAL PLACEMENT
Design style placement problems: Classification of placement algorithms, Simulation based placement algorithms and Partitioning based placement algorithms. Timing-driven placement.

UNIT-IV
GLOBAL ROUTING
Design Style specific global routing problems, classification of global routing algorithms, Maze routing algorithms, Line-Probe algorithms. Via Minimization - Constrained and unconstrained via minimization - Constrained and unconstrained via minimizations.

UNIT-V
CELL ROUTING
Single layer and two-layer routing, Clock Routing : Clocking Schemes, Design consideration for the clocking systems, problem formulation, Clock routing algorithms, Skew and delay reduction by pin assignment, multiple clock routing. Power Routing, Compaction algorithms - style specific compaction problem, classification of compaction algorithms, one-dimension compaction.

TEXT BOOKS

1. S.H.Gerez, Algorithms for VLSI Design Automation, WILEY student Edition, John Wiley& (Asia) Pvt. Ltd. 1999.

2. Naveed Sherwani, Algorithms for VLSI Physical Design Automation, Springer International Edition 3rd edition, 2005.

REFERENCES

1. Hill & Peterson, Computer Aided Logical Design with Emphasis on VLSI, John Wile, 1993.

2. Wayne Wolf, Modern VLSI Design: Systems on silicon, Pearson Education Asia, 2nd Edition, 1998.

Elective-III
MEMORY TECHNOLOGIES
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE2.3	**L**	**P**	**C**
II-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course, the student will be able to:
CO1: Summarize Static Random Access Memory Technologies.
CO2: Outline the concepts of dynamic random access memory technologies.
CO3: Demonstrate various nonvolatile memories
CO4: Illustrate Memory Reliability and Radiation Effects
CO5: Describe advanced memory technologies

UNIT-I
STATIC RAM TECHNOLOGIES
Static Random Access Memories (SRAMs), SRAM Cell Structures, MOSSRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT-II
DYNAMIC RAM TECHNOLOGIES
DRAMs, MOS DRAM Cell, Bi-CMOSDRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

UNIT-III
NON-VOLATILE MEMORIES
Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT-IV
MEMORY RELIABILITY AND RADIATION EFFECTS
General Reliability issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

UNIT-V
ADVANCED MEMORY TECHNOLOGIES
Introduction to memory technologies, High-density Memory Packing Technologies, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

TEXT BOOKS

Ashok K Sharma, Advance Semiconductor Memories: "Architectures, Designs and Applications", Wiley.

REFERENCES

1. Kiyoo Itoh, VLSI memory chip design, Springer International Edition
2. Ashok K Sharma, Semiconductor Memories: Technology, Testing and Reliability, PHI

Elective-III
SoC DESIGN
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE2.3	**L**	**P**	**C**
II-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course, the student will be able to:
CO1: Illustrate SoC based design.
CO2: Describe the NISC modeling
CO3: Differentiate simulation models
CO4: Analyze low power concepts
CO5: Apply synthesis optimization techniques

UNIT-I
ASIC DESIGN METHODOLOGIES
Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC, Architectural issues and its impact on Soc design methodologies, Application Specific Instruction Professor (ASIP) concepts.

UNIT-II
NISC DESIGN FLOW
NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)-design flow, modeling NISC Architectures and systems.

UNIT-III
SoC SIMULATION METHODOLOGY
Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact.

UNIT-IV
LOW POWER SoC DESIGN
Digital system, Design synergy, Low Power system perspective-power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, power down techniques.

UNIT-V
SYNTHESIS
Role and Concept of graph theory and its relevance to synthesize able constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization,

Constraints, Synthesis report analysis single core systems, HDL coding techniques for minimization of power consumption.

TEXT BOOKS

Hubert Kaeslin, Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication, Cambridge University Press, 2008.

REFERENCES

1. B. Al Hashimi, System on chip-Next generation electronics, The IET, 2006.
2. Rochit Rajsuman, System-on-a-chip: Design and test, Advantest America R & D Center, 2000.
3. P Mishra and N Dutt, Processor Description Languages, Morgan Kaufmann, 2008.
4. Michael J. Flynn and Wayne Luk, Computer System Design: System-on-Chip. Wiley, 2011.

Elective-IV
LOW POWER VLSI DESIGN
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE2.4	**L**	**P**	**C**
II-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course, the student will be able to:
CO1: Describe the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
CO2: Explain the different approaches of Low power design at circuit level
CO3: Summarize the different approaches of low power clock distribution.
CO4: Model power consumption & understand the basic analysis Methods.
CO5: Discuss the Low-Power Memories and Basics of DRAM.

UNIT-I
TECHNOLOGY & CIRCUIT DESIGN LEVELS
Sources of power dissipation in digital ICs, Degree of freedom, Recurring themes in low-power, Emerging low power approaches, Dynamic dissipation in CMOS, effects of V_{dd} and V_t on speed, Constraints on V_t reduction, Transistor sizing and optimal gate oxide thickness, Impact of technology scaling, Technology innovations.

UNIT-II
LOW POWER CIRCUIT TECHNIQUES
Power consumption in circuits, flip-flops and latches, high capacitance nodes. Energy recovery CMOS: Reversible pipelines, high performance approaches.

UNIT-III
LOW POWER CLOCK DISTRIBUTION
Power dissipation in clock distribution, Single driver versus distributed buffers, Buffers and device sizing under process variations, Zero skew Vs. Tolerable skew, Chip and package co-design of clock network.

UNIT-IV
LOW POWER ESTIMATION TECHNIQUES
Logic Synthesis for Low Power: Power Estimation Techniques, Power minimization techniques. Low power arithmetic components: Circuit design styles, Address and Multipliers.

UNIT-V
LOW POWER MEMORY DESIGN
Sources and Reduction of Power Dissipation in Memory subsystem, Sources of power dissipation in DRAM and SRAM, Low power DRAM circuits, Low power SRAM Circuits.

TEXT BOOKS

1. P. Rashinkar, Paterson and L. Singh, Low Power Design Methodologies, Kluwer Academic, 2002.
2. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits – Analysis and Design, TMH, 2011.

REFERENCES

1. Kaushik Roy, Sharat Prasad, Low Power CMOS VLSI circuit design, John Wiley sons Inc., 2000.
2. J.B. Kulo and J.H. Lou, Low voltage CMOS VLSI Circuits, Wiley, 1999.
3. A.P. Chandrasekaran and R. W. Broadersen, Low power digital CMOS Design, Kluwer, 1995.
4. Kiat-Seng Yeo, Kaushik Roy, Low-voltage, Low-Power VLSI Subsystems, TMH Professional Engineering.

Elective-IV
DSP ARCHITECTURE
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE2.4	**L**	**P**	**C**
II-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course, the student will be able to:
CO1: Differentiate between DSP processor and General purpose microprocessor.
CO2: Understand basic architectural features required in a Digital signal Processor.
CO3: Understand the use of very large instruction word architecture in achieving high Performance through increased instruction parallelism.
CO4: Design and implement various signal processing algorithms using 6X Series Processor.
CO5: Design of various blocks of radio receiver using digital hardware.

UNIT-I
INTRODUCTION TO DSP PROCESSORS
Difference between DSP Processor and General purpose microprocessor architecture. Computational accuracy in DSP implementations: fixed point format, floating point format, sources of error in DSP implementation, A/D conversion errors, DSP computational errors, D/A conversion errors, Basic TMS320 architectures.

UNIT-II
BASIC ARCHITECTURAL FEATURES OF DSP DEVICES
MAC unit, Barrel shifters, Bus architecture and Memory, Data addressing capabilities, Address generation unit, Programmability and Program execution, Speed issues, Hardware looping, Interrupts, Stacks, Relative support, Pipelining and performance, Pipeline depth, Interlocking, Branching, effects, interrupt effects, Pipeline programming models.

UNIT-III
VLIW ARCHITECTURE
TMS320C6X architecture and Instruction set, Pipelining, Addressing modes, Timers, Interrupts, Multichannel Buffered Serial Ports, Direct memory access, Code composer studio.

UNIT-IV
IMPLEMENTATION OF BASIC DSP ALGORITHMS
FIR filter implementation: Band stop & Band pass, Effects of voice using three FIR low pass filters, FIR implementation with pseudorandom noise sequence as input to filter, IIR filter implementation using second order Difference equations, DFT of as sequence of real numbers, FFT of a real time input signal.

UNIT-V
FPGA BASED DSP SYSTEMS
Evolution of FPGA based DSP system design, Introduction to FPGA, Design flow, for and FPGA based system design, CAD tools for FPGA based system design, Soft-core processors,

FPGA based DSP system design. FPGA's in Telecommunication applications- Coordinate rotation Digital Computer (CORDIC) algorithms and its applications, Case study of an FPGA based Digital receiver.

TEXT BOOKS

1. Avatar Singh and S. Srinivasan, Digital Signal Processing, Thomson Publications, 2004.
2. B. Venkata Ramani and M. Bhaskar, Digital signal Processors, Architecture, Programming and applications, Tata Mc graw Hill, 2004.
3. Rulph Chassaing, Digital Signal Processing and Applications with the TMS320C6713 and TMS320C6416 DSK, Second edition, John Wiley & Sons, 2011

REFERENCES

Uwe Meyer-Baese, Digital Signal Processing with Field Programmable Gate Arrays, 4th edition, Springer Publications, 2014.

Elective-IV
ANALOG AND DIGITAL CMOS VLSI DESIGN
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE2.4	**L**	**P**	**C**
II-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Analyze the depth of designing a Digital IC and use the concept of logical effort for Transistor sizing.
CO2: Describe the static and dynamic behavior of CMOS.
CO3: Differentiate Static CMOS design and Dynamic CMOS design.
CO4: Analyze small signal modeling of single stage MOSFET amplifier with current mirrors.
CO5: Design two stage CMOS operational amplifiers and illustrate advance current mirrors.

UNIT-I
REVIEW OF MOS STRUCTURES
Basic MOS structure and its static behavior, Quality metrics of a digital design, Cost, Functionality, Robustness. Power and Delay, Stick diagram and Layout, Wire delay models. Inverter: static CMOS inverter, switching threshold and noise margin concepts and their Evaluation, Dynamic behavior, Power consumption.

UNIT-II
PHYSICAL DESIGN FLOW
Floor planning, placement, Routing, CTS, Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, cascading dynamic gates logic.

UNIT-III
SEQUENTIAL LOGIC
Static latches and registers, Bi-stability principle, MUX based latches, Static SR Flipflops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of Pipelining Pulse registers, and Non-bis-table sequential circuit.

UNIT-IV
CURRENT MIRRORS AND OP-AMPS
Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise, Operational amplifiers: One stage OPAMP, two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR.

UNIT-V
DESIGN OF AMPLIFIERS
CS stage with resistance load, Divide connected load, Current source load, Triode Load, CS stage with source degeneration, Source follower, Common gate stage, Cascade stage, Choice

of device models, differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

TEXT BOOKS

1. Rabacy, Jan M, Anantha P.Chandrakasan, and Borivoje Nikolic. Digital Integrated Circuits, 2nd Edition, Engle wood Clifts: Prentice hall, 2002.
2. Behzd Razavi, Design of Analog CMOS Integrated Circuits, TMH, 2007.
3. D.A.John & Ken Martin, Analog Integrated Circuit Design, John Wiley, 1997.

REFERENCES

1. Allen, Philip E., and Douglas R. Holberg, CMOS analog circuit design, 3rd Edition. Elsevier. 2011.
2. Leblebici, Yusuf, CMOS digital integrated circuits: analysis and design. 3rd Edition. McGraw-Hill College, 1996
3. Baker, R. Jacob. CMOS: circuit design layout, and simulation. Wiley-IEEE press, 2019.

MTVE 2.5 Audit course
(Refer Annexure-I for Syllabus Details)

VLSI DESIGN VERIFICATIN AND TESTING LAB
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE2.6	**L**	**P**	**C**
II-Semester	**0**	**3**	**2**
	Ext. Marks:----		
	Int. Marks: 100		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Develop packet, class, driver, mailbox, and score board for a DUT
CO2: Test polymorphism with DUT
CO3: Analyze line, code and functional coverage
CO4: Examine the assertions for DUT
CO5: Develop semaphores for test-bench

LIST OF EXPERIMENTS:
1. Implementation of packet and class for a simple DUT
2. Implementation of driver for a simple DUT
3. Implementation of mailbox for a simple DUT
4. Implementation of scoreboard for a simple DUT
5. Testing of polymorphism with DUT
6. Line and Code coverage of counter
7. Line and Code coverage of FIFO
8. Line and Code coverage of FSM
9. Functional coverage and Code coverage of ALU
10. Functional coverage and Code coverage of UART
11. Assertions for a simple DUT
12. Implementation and testing of semaphore of ALU model
13. Implementation and testing of semaphore for a read/writer from a memory
14. Bus Function Model Generation & Testing for a simple DUT

Note: Any **TWELVE** of the above experiments are to be conducted.

ANALOG AND DIGITAL CMOS VLSI DESIGN LAB
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE2.7	**L**	**P**	**C**
II-Semester	**0**	**3**	**2**
	Ext. Marks:----		
	Int. Marks: 100		

COURSE OUTCOMES: At the end of the course the student will be able to:
CO1: Analyze VI Characteristics NMOS and PMOS Devices.
CO2: Analyze Voltage transfer characteristics of CMOS inverter.
CO3: Demonstrate transient and AC analysis of CMOS inverter.
CO4: Calculate small signal voltage gain of CS amplifier.
CO5: Design the layout of a minimum size inverter.

LIST OF EXPERIMENTS:

1. To the given parameters of a CMOS Process

i. Plot I_D vs. V_{GS} at different drain voltages for NMOS, PMOS

ii. Plot I_D vs. V_{GS} at different drain voltages (low) for NMOS, PMOS and determine Vt

iii. Plot log I_D vs. V_{GS} at different gate voltages (high) for NMOS, PMOS and determine OFF and sub-threshold slope.

iv. Plot I_D vs. V_{DS} at different gate voltages for NMOS, PMOS and determine Channel Length Modulation factor.

2. To the given parameters of a CMOS Process, Extract Vth of NMOS/PMOS transistors (short channel and long channel).

i. Plot g_m vs. V_{GS} and obtain peak gm point.

ii. Plot $y=I_D/ g_m$ as a function of V_{GS}.

iii. Plot tangent line passing through peak gm point in y (V_{GS}) plane and determine Vth.

3. To the given parameters of a CMOS Process, Plot I_D vs. V_{DS} at different drain voltages for NMOS, PMOS, Plot DC load line and calculate g_m, g_{ds}, g_m/g_{ds}, and unity gain frequency. Tabulate your result according to technologies and comment on it.

4. To the given parameters of a CMOS Process, Perform the following

i. Plot VTC curve for CMOS inverter and there on plot dV_{out} vs. dV_{in} and determine Transition Voltage and gain g. Calculate $V_{IL,}V_{IH,}$ $NM_{H,}$ NM_L for the Inverter.

ii. Plot VTC for CMOS inverter with varying V_{DD}

iii. Plot VTC for CMOS inverter with varying device ratio.

5. Perform transient analysis of CMOS inverter with no load and with load and determine $T_{PHL,}$ $T_{PLH.}$

6. Perform AC analysis of CMOS inverter with fanout-0 and fanout-1.

7. Design three stage and five stages ring Oscillator circuits and compare their frequencies and the time periods.

8. Draw small signal voltage gain of the minimum size inverter for specified technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point.

9. Consider a small CS amplifier with active load with NMOS transistor M_N as driver and PMOS transistor M_P as load, in specified technology to achieve $V_{DSQ}=V_{DD}/2$.
i. Calculate input bias voltage.
ii. Obtain the bias Current.

10. Consider a small CS amplifier with active load with NMOS transistor M_N as driver and PMOS transistor M_P as load, in specified technology.
i. Determine small signal voltage,-3db BW and GBW of the amplifier using small signal analysis.
ii. Plot step response of the amplifier for input. Derive time constant of the output and compare it with the time constant resulted from -3db BW
iii. Determine input voltage range of the amplifier.

11. Consider a simple CD amplifier with active load with NMOS transistor M_N as a driver and PMOS transistor M_P as load, in specified technology to achieve $V_{DSQ}=V_{DD}/2$.
i. Calculate input bias voltage.
ii. Obtain the bias current.

12. Consider a simple CD amplifier with active load with NMOS transistor M_N as a driver and PMOS transistor M_P as load, in specified technology.
i. Determine small signal voltage, -3db BW and GBW of the amplifier using small signal analysis.
ii. Plot step response of the amplifier for input. Derive time constant of the output and compare it with the time constant resulted form of -3db BW
iii. Determine input voltage range of the amplifier.

13. Design a differential amplifier and perform transient and AC analysis for the specified technology.

14. For the specified technology draw the layout of a minimum size inverter. Run DRC, LVS and RC extraction.

NOTE: ANY **TWELVE** of the above experiments are to be conducted.

MINI PROJECT WITH SEMINAR

Elective -V
OPTIMIZATION TECHNIQUES
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE3.1	**L**	**P**	**C**
III-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of this course, the student will be able to
CO1: Comprehend the techniques and applications of engineering optimization.
CO2: Analyze characteristics of a general linear programming problem
CO3: Apply basic concepts of mathematics to formulate an optimization problem
CO4: Analyze various methods of solving the unconstrained minimization problem
CO5: Analyze and appreciate variety of performance measures for various optimization problems

UNIT-I
INTRODUCTION TO OPTIMIZATION
Introduction to Classical Methods & Linear Programming Problems Terminology, Design Variables, Constraints, Objective Function, Problem Formulation. Calculus method. Kuhn Tucker conditions, Method of Multipliers.

UNIT-II
LINEAR PROGRAMMING PROBLEM
Linear Programming Problem, Simplex method, Two-Phase method, Big-M method, duality, Integer linear Programming, Dynamic Programming, Sensitivity analysis.

UNIT- III
SINGLE VARIABLE OPTIMIZATION PROBLEMS
Optimality Criterion, Bracketing Methods, Region Elimination Methods, Interval Halving Method, Fibonacci Search Method, Golden Section Method. Gradient Based Methods: Newton-Rap son Method, Bisection Method, Secant Method, Cubic search method.

UNIT- IV
MULTIVARIABLE AND CONSTRAINED OPTIMIZATION TECHNIQUES
Multivariable and Constrained Optimization Technique, Optimality Criteria, Direct search Method, Simplex search Methods, Hooke-Jeeve's pattern search method, Powell's conjugate direction method, Gradient based method, Cauchy's Steepest descent method. Newton's method, Conjugate gradient method. Kuhn-Tucker conditions, Penalty Function, Concept of Lagrangian multiplier, Complex search method, Random search method

UNIT- V
INTELLIGENT OPTIMIZATION TECHNIQUES
Introduction to Intelligent Optimization, Generic Algorithm: Types of reproduction operators, crossover & mutation, Simulated Annealing Algorithm, Particle Swarm Optimization (PSO), Genetic

Programming (GP): Principles of genetic programming, terminal sets, functional sets, differences between GA & GP, random population generation, solving differential equations using GP.

TEXTBOOKS

1. S.S.Rao, Engineering Optimization: Theory and Practice, Wiley, 2008.
2. K.Deb, Optimization for Engineering design algorithms and Examples, Practice Hall, 2nd edition 2012.

REFERENCES

1. C.J.Ray, Optimum Design Mechanical Elements, Wiley, 2007.
2. R. Saravanan, Manufacturing Optimization through Intelligent Techniques, Taylor & Francis Publications, 2006.
3. D.E. Goldberg, Genetic algorithms in Search Optimization, and Machine Learning, Addison-Wesley Longman Publishing, 1989.

Elective -V
BIOMEDICAL SIGNAL PROCESSING
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE3.1	**L**	**P**	**C**
III-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of this course, the student will be able to
CO1: Understand different types of biomedical signals.
CO2: Understand the acquisition of various biomedical signals.
CO3: Analyze then on-stationary biomedical signals in spectral domain using wavelet transform.
CO4: Analyze the chaotic signals using various orthogonal transformation techniques.
CO5: Understand biomedical signal classification using pattern recognition techniques.

UNIT-I
INTRODUCTION TO BIOMEDICAL SIGNAL PROCESSING
Acquisition, Generation of Bio-Signals, Origin of bio-signals, Types of bio-signals, Study of diagnostically significant bio-signal parameters.

UNIT-II
ELECTRODES FOR BIO-PHYSIOLOGICAL SENSING AND CONDITIONING
Electrode-electrolyte interface, polarization, electrode skin interface and motion arte fact, biomaterial used for electrode, Type of electrodes (body surface, internal, array of electrodes, microelectrodes), practical aspects of using electrodes, Acquisition of bio-signals (signal conditioning) and Signal conversion (ADC's DAC's) Processing.

UNIT-III
TRANSFORM TECHNIQUES
Biomedical Signal Processing by Fourier analysis, biomedical signal processing by wavelet (time frequency) analysis, Analysis (Computation of signal parameters that are diagnostically random signals and non-stationary signals,

UNIT-IV
DIMENSIONALITY REDUCTION TECHNIQUES
Principal Component analysis, Correlation and regression, Analysis of chaotic signals Application areas of Bio-Signals analysis Multiresolution analysis (MRA) and wavelets, Principal component analysis (PCA), Independent component analysis (ICA)

UNIT-V
PATTERN CLASSIFICATION
Supervised and unsupervised classification, neural networks, Support vector Machines, Hidden Markov models. Examples of biomedical signal classification examples.

TEXT BOOKS
1. R.M. Rangayyan Biomedical Signal analysis: A case study approach, IEEE press, John Wiley & Sons. Inc, 2002.

2. C. Raja Rao, SK Guha, Principles of Medical Electronics and Biomedical instrumentation, Universities Press, 2001.

REFERENCES

1. W. J. Tompkins, biomedical Digital signal Processing, Prentice Hall, 1993.
2. Eugene N Bruce, Biomedical Signal Processing and Signal Modeling, John Wiley & Son's publication, 2001.
3. D C Reddy, Biomedical Signal Processing, Mc Graw Hill, 2005.
4. Duda, R. O., Hart, P.E. and stroke, D.G., Pattern classification, John Wiley & sons, 2012.

Elective -V
INTERNET OF THINGS AND APPLICATIONS
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE3.1	**L**	**P**	**C**
III-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course, the student will be able to
CO1: Understand the fundamentals and application areas of IoT.
CO2: Illustrate the differences between IoT and M2M.
CO3: Discuss file handling, fate operations, and classes.
CO4: Build basic IoT applications using Raspberry Pi board.
CO5: Develop IoT infrastructure for smart application

UNIT-I
INTRODUCTION TO IoT
Introduction to Internet of Things, Physical Design of IoT, Logical Design of IoT, IoT Enabling Technologies, IoT Levels and deployment templates.

UNIT-II
M2M TO IoT
Introduction, M2M difference between IoT and M2M, SDN and NFV for IoT. Sensors, Participatory sensing, RFIDs, and Wireless sensor Networks: Sensor technology, participatory sensing, industrial IoT, automotive IoT, actuator, sensor data communication protocols, radio frequency identification technology, wireless sensor networks technology.

UNIT-III
IoT PLATFORMS DESIGN METHODOLOGY
IoT design methodology, motivation for using python, python data types & data structures, control flow, functions, modules, packages, file handling, date/time operations, classes, python packages of interest for IoT.

UNIT-IV
IoT PHYSICAL DEVICES & ENDPOINTS
Block diagram of basic IoT device, Raspberry pi, Linux on Raspberry pi, interfaces, programming Raspberry pi with python, other IoT devices.

UNIT-V
IoT PHYSICAL SERVICES AND CLOUD OFFERINGS
Introduction to cloud storage models and communication APIs, WAMP – Autobahn for IoT, Xively, cloud for IoT, Amazon Web services for IoT, case studies illustrating IoT design – home automation, smart cities, smart environment.

TEXTBOOKS
1. Arshdeep Bahga, Vijay Madisetti, Internet of Things – A hands – on approach, Universities Press, 2015.
2. Jan Ho”ller, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan.

3. Avesand. David Boyle, From Machine-to-Machine to the Internet of Things-Introduction to a New Age of Intelligence, Elsevier, 2014.(UNIT-II).
4. Raj Kamal, Internet of Things architecture and design principles McGrawHill Publications, 2017.

REFERENCES

1. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, IoT Fundamentals: Networking Technologies, Protocols and Use Cases for internet of Things, Cisco Press, 2017.
2. Dieter Uckelmann, Mark Harrison, Michahelles, Florian (Eds), Architecting the Internet of Things, Springer, 2011.

Open Elective
WASTE AS A SOURCE OF ENERGY
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE3.2	**L**	**P**	**C**
III-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course the student will be able to
CO1: Differentiate and characterize different waste.
CO2: Recognize the various waste to energy conversion processes.
CO3: Explain the various biochemical conversion processes.
CO4: Explain the various thermochemical conversion processes.
CO5**:** Explain the various biomass processes to energy conversion.

UNIT-I
Characterization and classification of waste as fuel: agro based, forest residues, industrial waste, domestic waste, municipal solid waste.

UNIT-II
Waste to energy options: combustion (unprocessed and processed fuel) gasification, anaerobic digestion, fermentation, and pyrolysis.

UNIT-III
Energy from waste-Bio-chemical conversion: Anaerobic digestion of sewage and municipal wastes, direct combustion of MSW-refuse derived solid fuel, industrial waste, agro residues, anaerobic digestion, biogas production, land fill gas generation and utilization.

UNIT-IV
Energy from waste- thermochemical conversion: sources of energy generation, incineration, pyrolysis, gasification of waste using gasifies, briquetting, utilization and advantages of briquetting, environmental and health impacts of incineration; strategies for reducing environmental impacts.

UNIT-V
Biomass energy technologies: Biomass characterization (proximate and ultimate analysis), Biomass pyrolysis and gasification, Biofuels – biodiesel, bioethanol, Biobutanol, Algae and biofuels, Hydrogenation, Solvent extraction of hydrocarbons, Pellets and bricks of biomass, Biomass based thermal power plants, Biomass as boiler fuel.

TEXT BOOKS:
1. Desai Ashok V, Non-Conventional Energy, Wiley Eastern Ltd, 1980.
2. Pichtel John, Waste management Practices Muncipal, Hazardous and Industrial, Taylor & Francis, 2005.

Open Elective
OPERATIONS RESEARCH
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE3.2	**L**	**P**	**C**
III-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course, the student will be able to
CO1: Formulate a linear programming problem for given problem and solve this problem by using simplex techniques.
CO2: Evaluate sensitivity analysis to the given input data in order to know sensitive of the output.
CO3: Apply the concept of non- linear programming for solving the problems involving non-linear constraints and objectives.
CO4: Solve deterministic and probabilistic inventory control models for known and unknown demand of the items.
CO5: Apply the dynamic programming to solve problems of discrete and continuous variables.

UNIT-I
Optimization techniques, model formulation, models, simplex techniques, inventory control models.

UNIT-II
Formulation of a LPP – graphical solution for LPP, revised simplex method – duality theory – dual simplex method – sensitivity analysis – parametric programming

UNIT-III

Nonlinear programming problem-Kuhn-Tucker conditions, CPM/PERT

UNIT-IV
Single server and multiple server models – deterministic inventory models – probabilistic inventory control models – geometric programming

UNIT-V
Single and multi-channel problems, sequencing models, dynamic programming, flow in networks, elementary graph theory, game theory simulation.

TEXTBOOKS
1. Kanthi Swarup, P.K. Gupta, Operations Research, 14th Edition Sultan Chand and sons, Delhi, 2008
2. S. D. Sharma, Operations Research, Kedar Nath and Ram Nath, Meerut, 2008.

REFERENCES
1. H. A.Taha, Operations Research, an Introduction, 7th Edition, PHI, 2008.
2. J. C. Pant, Introduction to Optimisation: Operations Research, 7th Edition, Jain Bros, Delhi, 2008.
3. Hitler Liebermann, Operations Research, Mc Graw Hill Pub., 2009.
4. Pannerselvam, Operations Research, Prentice Hall of India, 2010.
5. Harvey M Wagner, Principles of V Prentice Hall of India, 2010.

Open Elective
COMPOSITE MATERIALS
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE3.2	**L**	**P**	**C**
III-Semester	**3**	**0**	**3**
	Ext. Marks:70		
	Int. Marks: 30		

COURSE OUTCOMES: At the end of the course, the student will be able to

CO1: Explain the advantages and applications of composite materials.

CO2: Describe the properties of various reinforcements of composite materials.

CO3: Summarize the manufacture of metal matrix, ceramic matrix and C-C composites.

CO4: Describe the manufacture of polymer matrix composites.

CO5: Formulate the failure theories of composite materials.

UNIT-I

INTRODUCTION:

Definition – Classification and characteristics of Composite materials. Applications of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT-II

REINFORCEMENTS:

Preparation- layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and born fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures, iso-strain and iso-stress conditions.

UNIT-III

MANUFACTURING OF METAL MATRIX COMPOSITES:

Casting – Solid State diffusion technique, Cladding –Hot iso static pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid Phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving, Properties and applications.

UNIT-IV

MANUFACTURING OF POLYMER MATRIX COMPOSITES:

Preparation of Molding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression molding – Reaction injection molding. Properties and applications.

UNIT-V

STRENGTH: LAMINAR FAILURE CRITERIA

Strength ratio, maximum stress criteria, maximum strain criteria, interaction failure criteria, hygro thermal failure. Laminate first play failure-insight strength: Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots: stress concentrations.

TEXT BOOKS:

1. R.W.Cahn, Material Science and Technology – Vol 13- Composites, West Germany, 1994.
2. W D Callister, Jr., Adapted by R. Balasubramaniam, Materials Science and Engineering, John Wiley & Sons, NY, Indian edition, 2007.

REFERENCE BOOKS:

1. K.K. Chawla, Composite Materials, 3rd Edition, springer, 2012.
2. Deborah D.L. Chung, Composite Materials Science and Applications, 2nd Edition, springer, 2010.

DISSERTATION-I / INDUSTRIAL PROJECT
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE3.3	**L**	**P**	**C**
III-Semester	**0**	**0**	**10**
	Ext. Marks:---		
	Int. Marks: 100		

DISSERTATION-I / INDUSTRIAL PROJECT

DISSERTATION -II
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVE4.1	**L**	**P**	**C**
IV-Semester	**0**	**0**	**16**
	Ext. Marks:		**100**
	Int. Marks:		**----**

COURSE OUTCOMES:

CO 1: Apply critical and creative thinking in the design of engineering projects, plan and manage your time effectively as a team.

CO 2: Consider the business context and commercial positioning of designed devices or systems and apply knowledge of the real-world situations that a professional engineer can encounter.

CO 3: Use fundamental knowledge and skills in engineering and apply it effectively on a project and design and develop a functional product prototype while working in a team.

CO 4: Undertake an engineering project under mentorship and timely reflect on your own and peer's technical and non- technical learning.

CO 5: Orally present and demonstrate your product to peers, academics, general industry community and manage any disputes and conflicts within and outside your team.

ANNEXURE- I

AUDIT COURSE
ENLISH FOR RESEARCH PAPER WRITING
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVL1.6 & MTVL2.5	**L**	**P**	**C**
Semester-I & II	**3**	**0**	**0**

Ext. Marks:----

Int. Marks: 100

1. Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.
2. Clarifying Who Did What, Highlighting Your Finding, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction.
3. Review of the Literature, Methods, Results, Discussion, Conclusions, the Final Check.
4. Key skills are needed when writing a Title, key skills are needed when writing an abstract, key kills are needed when writing an Introduction, skills needed when writing a Review of the Literature.
5. Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, and skills are needed when writing the Conclusions.
6. Useful phrases, how to ensure paper is as good as it could possibly be the first-time Submission.

REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press.
3. Highman N (1998). Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

AUDIT COURSE
DISASTER MANAGEMENT
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVL1.6 & MTVL2.5	**L**	**P**	**C**
Semester-I & II	**3**	**0**	**0**
	Ext. Marks:----		
	Int. Marks: 100		

1. INTRODUCTION: DISASTER:
Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

2. REPERCUSSIONS OF DISASTERS AND HAZARDS:
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Manmade disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

3. DISASTER PRONE AREAS IN INDIA:
Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides and Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.

4. DISASTER PREPAREDNESS AND MANAGEMENT PREPAREDNESS:
Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk; Application of Remote Sensing, Data From Meteorological and other Agencies, Media Reports: Governmental and Community Preparedness.

5. RISK ASSESSMENT DISASTER RISK:
Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

6. DISASTER MITIGATION MEANING,
Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

REFERENCES:
1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "New Royal book Company.
2. Sahni, Paradeep Et.Al. (Eds.)" Disaster Mitigation Experience and Reflections", Prentice Hallf India, New Delhi.
3. Goel S.L., Disaster Administration and Management Text and case Studies", Deep & Deep Publication Pvt.Ltd. New Delhi

AUDIT COURSE
SANSKRIT FOR TECHNICAL KNOWLEDGE
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVL1.6 & MTVL2.5	**L**	**P**	**C**
Semester-I & II	**3**	**0**	**0**
	Ext. Marks:----		
	Int. Marks: 100		

1. Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences
2. Order Introduction of roots, Technical information about Sanskrit Literature
3. Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics.

REFERENCES:

1. "Abhayspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi.
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication.
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

AUDIT COURSE
VALUE EDUCATION
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVL1.6 & MTVL2.5	**L**	**P**	**C**
Semester-I & II	**3**	**0**	**0**

Ext. Marks:----

Int. Marks: 100

1. VALUES AND SELF –DEVELOPMENT –SOCIAL VALUES AND INDIVIDUAL ATTITUDES.
Work ethics, Indian vision of humanism.
Moral and non-moral valuation. Standards and principles.
Value judgements

2. IMPORTANCE OF CULTIVATION OF VALUES.
Sense of duty. Devotion, Self-reliance. Confidence, Concentration.
Truthfulness, Cleanliness.
Honesty, Humanity. Power of faith, National Unity.
Patriotism. Love for nature, Discipline

3. PERSONALITY AND BEHAVIOR DEVELOPMENT – SOUL AND SCIENTIFIC ATTITUDE.
Positive Thinking. Integrity and discipline.
Punctuality, Love and Kindness.
Avoid fault Thinking.
Free from anger, Dignity of labor.
Universal brotherhood and religious tolerance.
True friendship.
Happiness Vs suffering, love for truth.
Aware of self-destructive habits.
Association and cooperation.
Doing best for saving nature

4. CHARACTER AND COMPETENCE – HOLY BOOKS Vs BLIND FAITH.
Self –management and Good health.
Science of reincarnation.
Equality, Nonviolence, Humility, Role of Women.
All religions and same message.
Mind your Mind, Self-control.

REFERENCES

1. Chakraborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

AUDIT COURSE
CONSTITUTION OF INDINA
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVL1.6 & MTVL2.5	**L**	**P**	**C**
Semester-I & II	**3**	**0**	**0**
	Ext. Marks:----		
	Int. Marks: 100		

1. HISTORY OF MAKING OF THE INDIAN CONSTITUTION:
History
Drafting Committee, (Composition &Working)

2. PHILOSOPHY OF THE INDIAN CONSTITUTION:
Preamble
Salient Features

3. CONTOURS OF CONSTITUTIONAL RIGHTS & DUTIES:
Fundamental Rights
Right to Equality
Right to Freedom
Right against Exploitation
Right to Freedom of Religion
Cultural and Educational Rights
Right to Constitutional Remedies
Directive Principles of State Policy
Fundamental Duties.

4. ORGANS OF GOVERNANCE:
Parliament
Composition
Qualifications and Disqualifications
Powers and Functions
Executive
President
Governor
Council of Ministers
Judiciary, Appointment and Transfer of Judges, Qualifications
Powers and Functions

5. LOCAL ADMINISTRATION:
District's Administration head : Role and Importance,
Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation.
Pachayati raj: Introduction, PRI: ZilaPachayat.

Elected officials and their roles, CEO ZilaPachayat: Position and role.
Block level: Organizational Hierarchy (Different departments),
Village level, Role of Elected and Appointed officials,
Importance of grass root democracy.

6. ELECTION COMMISSION:

Election Commission: Role and Functioning.
Chief Election Commissioner and Election Commissioners.
State Election Commission: Role and Functioning.
Institute and Bodies for the Welfare of SC/ST/OBC and women.

REFERENCES

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S.N. Busi , Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M .P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D.Basu, Introduction to the Constitution of India, Lexis Nexis.

AUDIT COURSE
PEDAGOGY STUDIES
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVL1.6 & MTVL2.5	**L**	**P**	**C**
Semester-I & II	**3**	**0**	**0**

Ext. Marks:----

Int. Marks: 100

1. INTRODUCTION AND METHODOLOGY:
Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education.
Conceptual framework, Research questions.
Overview of Methodology and Searching.

2. THEMATIC OVERVIEW:
Pedagogical practices are being used by teachers in formal and informal
Classrooms in developing countries. Curriculum, Teacher education.

3. EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES
Methodology for the in depth stage: Quality assessment of included studies.
How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?
Theory of change.
Strength and nature of the body of evidence for effective pedagogical practices.
Pedagogic theory an pedagogical approaches.
Teachers' attitudes and beliefs and Pedagogic strategies.

4. PROFESSIONAL DEVELOPMENT:
Alignments with classroom practices and follow support Peer support.
Support from the head teacher and the community.
Curriculum and assessment.
Barriers to learning: limited resources and large class sizes.

5. RESEARCH GAPS AND FUTURE DIRECTIONS
Research design
Contexts
Pedagogy
Teacher education
Curriculum and assessment
Dissemination and research impact.

REFERENCES
1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana – does it count? Multi-site teacher education research project (MUSTER) country report, 1. London: DFID.4. Akyeampong K, Lussier K, Pryor

J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272-282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7.www.pratham.org/images/resource%20working%20paper%202.pdf

AUDIT COURSE
STRESS MANAGEMENT BY YOGA
(Effective from Admitted Batch of 2023-24)

Subject Code : MTVL1.6 & MTVL2.5	**L**	**P**	**C**
Semester-I & II	**3**	**0**	**0**
	Ext. Marks:----		
	Int. Marks: 100		

1. Definitions of Eight parts of yoga. (Ashtanga) 8
2. Yam and Niyam.

Do's and Don'ts in life.

i) Ahinsa, satya, astheya, bramhacharya and aparigraha

ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

3. Asan and Pranayam

i) Various yoga poses and their benefits for mind & body

ii) Regularization of breathing techniques and its effects-Types of pranayama

REFERENCES

1. 'Yogic Asanas for Group Training-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur.

2. "Raja yoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata.

AUDIT COURSE

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

(Effective from Admitted Batch of 2023-24)

Subject Code : MTVL1.6 & MTVL2.5	**L**	**P**	**C**
Semester-I & II	**3**	**0**	**0**
	Ext. Marks:----		
	Int. Marks: 100		

1. Neetisatakam-Holistic development of personality
Verses- 19, 20, 21, 22 (wisdom)
Verses- 29, 31, 32 (pride & heroism)
Verses- 26, 28, 63, 65 (virtue)
Verses- 52, 53, 59 (dont's)
Verses- 71, 73, 75, 78 (do's)

2. Approach to day to day work and duties.
Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47, 48.
Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5, 13, 17, 23, 35.
Chapter 18-Verses 45, 46, 48.

3. Statements of basic knowledge.
Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
Chapter 12 -Verses 13, 14, 15, 16, 17, 18
Personality of Role model. Shrimad Bhagwad Geeta:
Chapter2-Verses 17, Chapter 3-Verses 36, 37, 42,
Chapter 4-Verses 18, 38, 39 Chapter18 –
Verses 37, 38, 63

REFERENCES

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sasthanam, New Delhi.